CLAIMS:

1. A system comprising:

a centralized built-in self-test (BIST) controller that stores an algorithm for testing a plurality of memory modules, wherein the BIST controller stores the algorithm as a set of generalized commands that conform to a command protocol; and

a plurality of distributed sequencers that interpret the commands based on the command protocol and apply the generalized commands to the memory modules.

2. The system of claim 1, wherein the generalized commands specify the algorithm in accordance with the command protocol and without regard to timing requirements of the memory modules.

3. The system of claim 1, wherein the generalized commands specify the algorithm without regard to physical characteristics of the memory modules.

4. The system of claim 1, wherein each of the generalized commands includes a sequencer identifier that identifies one or more of the sequencers to process the respective command and apply the command to the memory modules.

5. The system of claim 4, wherein the sequencer identifier comprises a broadcast identifier to indicate that the generalized command is to be interpreted and applied by all of the distributed sequencers.

6. The system of claim 4, wherein the sequencer identifier comprises a unicast identifier that identifies a specific one of the sequencers to interpret and apply the generalized command to the respective memory modules of the identified sequencer.

7. The system of claim 4, wherein the command protocols defines each of the generalized commands to include an operational code selected from a set of defined operational codes and a set of associated parameters.

8. The system of claim 7, wherein the set of defined operational codes includes an operational code that directs the sequencers to selectively enable and disable a BIST mode during which the sequencers ready the memory modules for testing by isolating the memory modules from address and data lines used during normal operation.

9. The system of claim 7, wherein the set of defined operation codes includes an operational code that directs the sequencers to apply a sequence of one or more memory operations over a range of addresses specified by the parameters.

10. The system of claim 9, wherein the parameters include a single-row (SR) field to direct the sequencers to apply the memory operations for all columns of the memory module of the respective memory modules for the sequencers that has a largest column-bit option while maintaining a row address at zero.

11. The system of claim 9, wherein the parameters include an invert bits field to direct the sequencers to invert data defined by the parameters for each row and column matrix of the memory modules when applying the memory operations.

12. The system of claim 9, wherein the parameters include a rippling row field to direct the sequencers to apply the memory operations to the memory modules in a column-wise fashion by holding a column address for each of the memory modules constant and rippling a row address for each of the memory modules.

13. The system of claim 9, wherein the parameters include an invert rows field to direct the sequencers to invert data defined by the parameters for neighboring rows of the memory modules when applying the memory operations.

14. The system of claim 9, wherein the parameters include an invert columns field to direct the sequencers to invert data defined by the parameters for neighboring columns of the memory modules when applying the memory operations.

15. The system of claim 9, wherein the parameters include a plurality of operational fields to direct the sequencers to apply multiple memory operations to each of memory addresses of the memory modules.

16. The system of claim 9, wherein the parameters include a default data in field that directs the sequencers to apply an input data value to the memory modules during a read operation.

17. The system of claim 7, wherein the set of defined operation codes includes an operational code that directs the sequencers to execute a defined memory operation to a specific address specified by the parameters.

18. The system of claim 7, wherein the set of defined operational codes includes an operational code that directs the sequencers to test a particular one of the memory modules.

19. The system of claim 7, wherein the parameters include a failure analysis field to direct the sequencers to selectively toggle between a failure analysis mode and a BIST mode.

20. The system of claim 19, wherein when operating within the failure analysis mode a memory identification field of the parameters directs the sequencers to select data from a specific one of the memory modules for failure analysis and a bus slice field that indicates a portion of a multiplexed data bus from the selected memory module to be used for failure analysis.

21. The system of claim 7, wherein the set of defined operational codes includes an operational code that directs at least one of the distributed sequencers to apply a memory test algorithm stored within that sequencer.

22. The system of claim 1, further comprising a plurality of memory interfaces coupled between the sequencers and the memory modules, wherein the memory interfaces apply the commands to the memory modules under the direction of the sequencers and in accordance with physical characteristics of the memory module.

23. The system of claim 1, wherein BIST controller issues the commands to the sequencers in parallel for application to the memory modules.

24. The system of claim 1, wherein the sequencers apply the commands to the respective memory modules in accordance with timing requirements of the memory modules.

25. The system of claim 1, wherein each of the sequencers comprises:

a plurality of command controllers that implement the commands in accordance with a command protocol; and

a command parser to parse each of the commands to identify an operational code and a set of parameters based on the command protocol, wherein the command parser selectively invokes the command controllers based on the operational codes of the commands received from the BIST controller.

26. A device comprising:

centralized (BIST) control means for issuing commands that conform to a generalized command protocol and define a BIST algorithm for testing a plurality of distributed memory modules having different timing requirements and physical characteristics; and

distributed means for interpreting the commands and applying the commands to the memory modules in accordance with timing requirements and physical characteristics of the memory modules.

27. The device of claim 26, wherein the distributed means includes interface means for generating translated address and data signals based on the physical characteristics of the memory modules to apply the BIST algorithm to the memory modules.

28. A method comprising:

directing application of an algorithm from a centralized controller by issuing generalized commands that conform to a command protocol to test a plurality of memory modules; and

interpreting the commands with a distributed set of sequencers to apply the commands as one or more sequences of memory operations in accordance with the command protocol.

29. The method of claim 28, wherein the generalized commands specify the algorithm without regard to physical characteristics and timing requirements of the memory modules.

30. The method of claim 28, wherein directing application of the algorithm comprises issuing each of the commands to include a sequencer identifier that identifies one or more of the sequencers to process the command and apply the command to the respective memory modules.

31. The method of claim 30, wherein the sequencer identifier comprises one of a broadcast identifier indicating that the command is to be interpreted and applied by all of the distributed sequencers and a unicast identifier that identifies a specific one of the sequencers to interpret the command.

32. The method of claim 28, wherein directing application of the algorithm comprises issuing each of the commands to include an operational code selected from a set of defined operations codes and a set of associated parameters.

33. The method of claim 32, wherein the set of defined operational codes includes an operational code that directs the sequencers to selectively enable and disable a BIST mode during which the sequencers ready the memory modules for testing by isolating the memory modules from address and data lines used during normal operation.

34. The method of claim 32, wherein the set of defined operation codes includes an operational code that directs the sequencers to apply a sequence of one or more memory operations over a range of addresses specified by the parameters.

35. The method of claim 32, wherein the set of defined operation codes includes an operational code that directs the sequencers to execute a defined memory operation to a specific address specified by the parameters.

36. The method of claim 32, wherein the set of defined operation codes includes an operational code that directs the sequencers to test a particular one of the memory modules.

37. The system of claim 33, wherein the set of defined operational codes includes an operational code that directs at least one of the distributed sequencers to apply a memory test algorithm stored within that sequencer.

38. The method of claim 29, wherein issuing an algorithm comprises issuing the commands to the sequencers in parallel for application to the memory modules.